CODE OF CONDUCT FOR THE LABORATORY

- All students must observe the Dress Code while in the laboratory.
- Sandals or open-toed shoes are NOT allowed.
- Foods, drinks and smoking are NOT allowed.
- All bags must be left at the indicated place.
- The lab timetable must be strictly followed.
- Be PUNCTUAL for your laboratory session.
- Experiment must be completed within the given time.
- Noise must be kept to a minimum.
- Workspace must be kept clean and tidy at all time.
- Handle all equipments and components with care.
- All students are liable to pay for any damage to the equipment, accessories, tools, or components due to their own negligence.
- All equipments, apparatus, tools and components must be RETURNED to their original place after use.
- Students are strictly PROHIBITED from taking out any items from the laboratory.
- Students are NOT allowed to work alone in the laboratory without the Lab Supervisor
- Report immediately to the Lab Supervisor if any injury occurred.
- Report immediately to the Lab Supervisor any damages to equipment.

Before leaving the lab

- Place the stools under the lab bench.
- Turn off the power to all instruments.
- Turn off the main power switch to the lab bench.
- Please check the laboratory notice board regularly for updates.

GENERAL LABORATORY INSTRUCTIONS

You should be punctual for your laboratory session and should not leave the lab without the permission of the teacher.

Each student is expected to have his/her own lab book where they will take notes on the experiments as they are completed. The lab books will be checked at the end of each lab session. Lab notes are a primary source from which you will write your lab reports.

You and your partner will work closely on the experiments together. One partner doing all the work will not be tolerated. Both partners should be able to explain the purpose of the experiment and the underlying concepts.

Please report immediately to the member of staff or lab assistant present in the laboratory; if any equipment is faulty.

Organization of the Laboratory

It is important that the experiments are done according to the timetable and completed within the scheduled time.

You should complete the prelab work in advance and utilize the laboratory time for verification only.

The aim of these exercises is to develop your ability to understand, analyze and test them in the laboratory.

A member of staff and a Lab assistant will be available during scheduled laboratory sessions to provide assistance.

Always attempt experiments; first without seeking help. When you get into difficulty; ask for assistance.

Assessment

The laboratory work of a student will be evaluated continuously during the semester for 25 marks. Of the 25 marks, 15 marks will be awarded for day-to-day work. For each program marks are awarded under three heads**:**

- Prelab preparation – 5 marks
- Practical work – 5marks, and
- Record of the Experiment – 5marks

Internal lab test(s) conducted during the semester carries 10 marks.

End semester lab examination, conducted as per the JNTU regulations, carries 50 marks.

At the end of each laboratory session you must obtain the signature of the teacher along with the marks for the session out of 10 on the lab notebook.

Lab Reports

Note that, although students are encouraged to collaborate during lab, each must individually prepare a report and submit.

They must be organized, neat and legible.

Your report should be complete, thorough, understandable and literate.

You should include a well-drawn and labeled engineering schematic for each circuit investigated

Your reports should follow the prescribed format, to give your report structure and to make sure that you address all of the important points.

Graphics requiring drawn straight lines, should be done with a straight edge. Well drawn free-hand sketches are permissible for schematics.

Space must be provided in the flow of your discussion for any tables or figures. Do not collect figures and drawings in a single appendix at the end of the report.

Reports should be submitted within one week after completing a scheduled lab session.

Presentation

Experimental facts should always be given in the past tense.

Discussions or remarks about the presentation of data should mainly be in the present tense.

Discussion of results can be in both the present and past tenses, shifting back and forth from experimental facts to the presentation.

Any specific conclusions or deductions should be expressed in the past tense.

Report Format:

Lab write ups should consist of the following sections:

Objectives

Prelab work

Components and equipment

Circuit diagram

Observations

Postlab work

Conclusions

And

Answers to questions

LIST OF EXPERIMENTS

1. P-N Junction Diode Characteristics
2. Zener Diode Characteristics
3. Half Wave & Full Wave Rectifier Circuits without Filters
4. Half Wave & Full Wave Rectifier Circuits with Capacitor Filter
5. Transistor Common Base Characteristics
6. Transistor Common Emitter Characteristics
7. Junction Field Effect Transistor Characteristics
8. Single Stage Common Emitter BJT Amplifier
9. Single Stage Common Source JFET Amplifier
10. Common Collector BJT Amplifier
11. UJT Characteristics
12. SCR Characteristics

EXPERIMENT: 01

P-N JUNCTION DIODE CHARACTERISTICS

Objectives:

The objectives of this experiment are:

1. To plot the forward & reverse bias current vs voltage characteristics of a p-n junction silicon and germanium diodes.

2. To verify the diode equation.

3. To determine the mechanism factor, η ,value in the diode equation.

4. To calculate the static and dynamic resistance of the diode at a selected operating point on the characteristics.

5. To compare the characteristics of silicon and germanium diodes.

Pre lab

1. Study the data sheets of silicon diode, 1N4007 and the germanium diode, 0A79 and note the following in your observation book.

a)The anode and cathode identification

b) Maximum average forward current, I_{Fmax}

c) Maximum average forward voltage, V_{Fmax}

d) Maximum peak inverse voltage, PIV_{max}

e) Maximum reverse current at the room temperature, I_S

2. Sketch the diodes characteristics and mark the above parameters.

3. Write the diode equation governing the characteristic

4. Define static and dynamic resistance of a diode

5. Compare the performance parameters of Germanium and Silicon Diodes

Components and Equipment:

1. Resistors: Carbon type 470Ω, ½ W and 1MΩ, 1/4 W. 5% - One each

2. Diodes: Silicon 1N4007 and Germanium 0A79 – One each

3. Cables & wires – as required

4. Oscilloscope (CRO) - One

5. Digital Multimeters (DMM) - Two

6. Regulated DC Power Supply, 0-30V - One

7. Breadboard - One

Circuit Diagram:

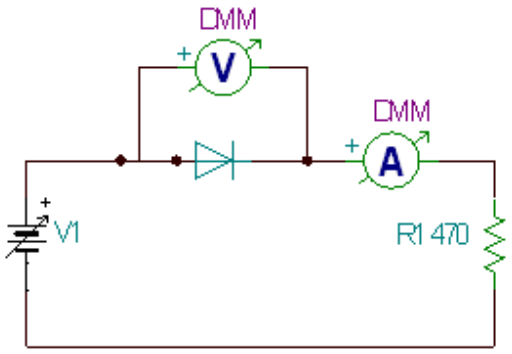


Fig 1.1 Forward Bias circuit

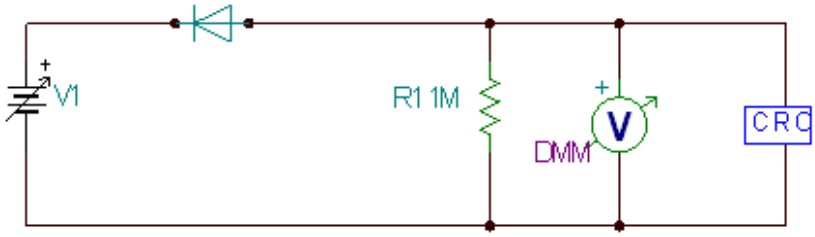


Fig 1.2 Reverse Bias circuit

Procedure:

1. Identify the anode and cathode for the diodes.
2. Test the diodes using DMM.
3. Note the colour code on the resistor and record the resistor type, value, Tolerance and wattage.
4. Measure the resistors with the DMM and record the Values.
5. Connect the Circuit in Fig1.1
6. Adjust the supply voltage V1, until the voltage drop V_D across the diode is 0.2V, 0.3V and so on, as given in the Table1.1a; measure and record V_D and I_D with the DMM.

Table 1.1a

V_D (mV)	200	300	400	500	600	625	650	675	700	710	720	730
I_D (mA)												

Note the diode voltage V_D at which I_D changes from Zero.

7. Replace the Silicon diode in the circuit with the Germanium diode, 0A79.
8. Repeat step-6 for the Germanium diode and tabulate the readings in Table 1.1b.

Table 1.1b

V_D	100	150	200	250	275	300	325	350	375	400	410	420
I_D (mA)												

Note the diode voltage V_D at which I_D changes from Zero.

9. Connect the circuit as in fig 1.2
10. Adjust the supply voltage until the voltage drop V_D across diode is -1V,-2V and so on, as given in Table 1.2; measure and record voltages across the diode and the resistor, V_D and $V_{R,}$ with the DMM and V_R with CRO also.

Table 1.2

V_D (V)	-1	-2	-3	-4	-5	-6	-7	-8	-9	-10
V_R (V) DMM										
$I_{S=}(V_{R1}/R1)\mu A$										
V_R (V) CRO										

11. Replace the Silicon diode in the circuit with the Germanium diode, 0A79.
12. Repeat step 10 for the Germanium diode and tabulate the readings.
13. Read the room temperature from the thermometer and note in the observation book.

Post Lab:

1. Plot the diode Current I_D vs voltage V_D for the Silicon and Germanium diodes.
2. Substitute $I_{D,}$ $V_{D,}$ I_S and T values in the diode equation and calculate the η value for four different readings, both for Silicon and Germanium diodes.
3. Verify diode equation plotting ln(I_D) vs V_D. The plot should fit into a straight-line.
4. From the graph in step 3 find the values of I_S and η, and compare with practically measured I_S value and η calculated in step2.
5. From the I_D vs V_D characteristics, note the cut-in voltage for the Silicon and Germanium diodes.
6. Calculate the static and dynamic resistances at I_D = 10mA for both the diodes from the characteristics (graph). Static resistance $R_F = (V_D / I_D)\ \Omega$, dynamic resistance $r_f = \Delta V_D / \Delta I_D$ at I_D = 10mA.
7. Compare the Germanium and Silicon diodes
8. Compare the readings with CRO & DMM in steps 10 & 12 and explain.
9. List the precautions you observed while performing the experiment.

Questions:

1. What happens when the reverse bias voltage exceeds the maximum rating of the peak inverse voltage?
2. What is the maximum power loss in the 470Ω resistor?
3. Can we use 1MΩ in fig 1.1 and 470Ω in fig1.2 and perform the experiment? If not, why?

EXPERIMENT: 02

ZENER DIODE CHARACTERISTICS

Objectives:

The objectives of this experiment are:

1. To plot the I-V characteristic curve of the Zener diode under reverse biased condition.
2. To calculate the dynamic resistance of the Zener diode in the break down region.
3. To study the Voltage regulation characteristic of the Zener diodes.

Pre lab

Study the data sheet of 1N4739 Zener diode and note the following in your observation book.

1) Nominal Zener Voltage Vz

2) Maximum Zener Current I_{ZM}

3) Maximum Power rating or dissipation P_D

4) The Knee Current I_{zk}

5) Maximum Zener impedance Z_{zk} at I_{zk}

6) Maximum Zener impedance Z_{zt} at the test Current I_{zt}

7) Sketch the Zener diode characteristic and mark the parameters V_{ZT}, I_{ZT}, V_{ZK}, and I_{ZM} on the characteristic.

Components and Equipment:

1. Resistors: Carbon type 470Ω, 1W and 1KΩ ,1/4 W. 5%
2. Zener Diode: 1N4739
3. Cables & wires
4. Digital Multi meter (DMM)-2
5. Regulated DC Power Supply, 0-30V, 1A
6. Bread Board

.

Circuit Diagram:

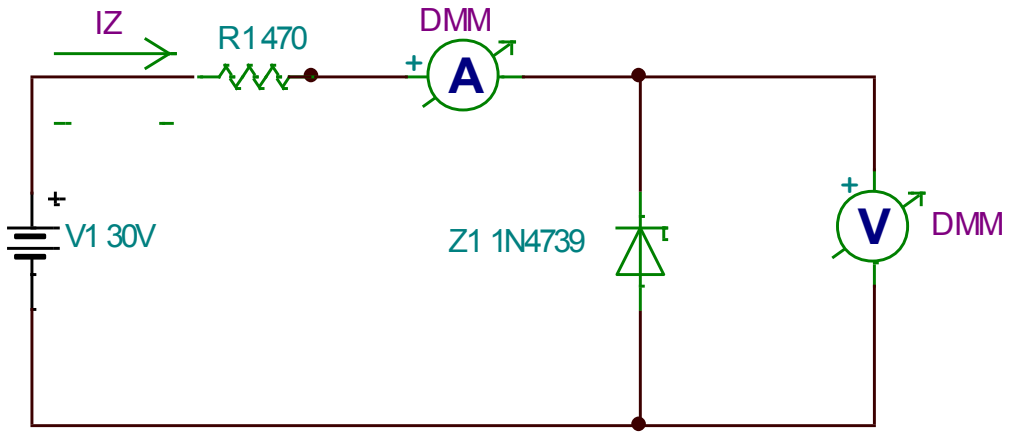


Fig 2.1 (a) Zener test circuit

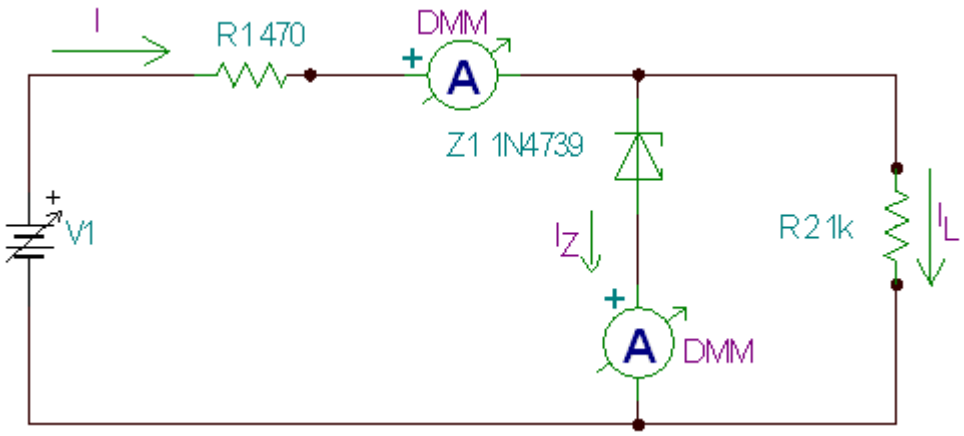


Fig 2.1 (b) Zener Regulator

Procedure:

Zener diode Characteristic:

1. Identify the anode and cathode for the diode.
2. Test the diode using DMM and CRO.
3. Note the colour code on the resistor and record the resistor type, value, tolerance and wattage.
4. Measure the resistors with the DMM and record the values.
5. Connect the Circuit in Fig2.1a.
6. Adjust the supply voltage V1 as given in the table 2.1; measure and record the Zener Voltage V_Z and Current Iz at each step.

Table 2.1

V1(v)	2	4	6	8	8.5	9.0	9.5	10	15	20	25	30
V_Z (v)												
I_Z(mA)												

Zener Regulator:

1. Connect the circuit of fig 2.1b.

2. Vary the supply Voltage V1 as given in Table 2.2. Measure and record V1, I, I_Z and V_Z at each step.

Table 2.2

V1(v)	6	8	9	10	12	15	20	25	30
I (mA)									
I_Z (mA)									
V_Z (V)									
$I_L = (V_z / R_L)$ mA ——									

Post Lab:

1. Plot the Zener voltage V_Z versus Zener Current I_Z, from the data in Table 2.1.V_Z and I_Z are negative values as the diode is operated in the reverse bias region.
2. From the plot determine V_{ZK} & I_{ZK} and V_{ZT} at I_{ZT}=10mA.
3. From the plot determine the dynamic resistance, $\Delta V_Z/\Delta I_Z$ of the Zener at I_{ZT}=20mA.
4. Plot the supply voltage V1 versus V_Z or V_L from the data in Table 2.2.
5. From the plot in step 4 calculate the

   Line Regulation %=($V_Z$max -$V_Z$min)/ (V1max – V1min) *100=($\Delta V_Z/\Delta$V1) * 100.
6. Compare the Zener diode and normal P-N junction diode characteristics.
7. List the precautions you observed while performing the experiment.

Questions:

1. What is the maximum power loss in 470Ω resistor in fig: 2.1a and fig: 2.1b?
2. What is the maximum power loss in the 1KΩ resistor in fig: 2.1b?
3. What is the maximum power loss in Zener diode in fig: 2.1a and fig: 2.1b?
4. What is the significance of the dynamic resistance of the Zener diode?
5. What did you notice from the Currents I, I_Z and I_L recorded in Table 2.2.

EXPERIMENT: 03

HALF WAVE & FULL WAVE RECTIFIER CIRCUITS WITHOUT FILTERS

Objectives:

To study the performance without filters, of

a) Half wave rectifier

b) Two diode full wave rectifier and

C) Bridge type full wave rectifier.

Pre lab:

1. Study the working of half wave & full wave bridge rectifiers and their performance parameters.
2. Study the data sheet of 1N4007 diode and note the maximum ratings.
3. Study the data sheet of W04M bridge rectifier and note the maximum ratings.

Components and Equipment:

1. Centre tapped step down 12-0-12V mains Transformer	-01 No
2. 1N4007 diodes	-02No
3. W04MBridge Rectifier	-01 No
4. Resistor: Carbon 1K,1/4W, 5%	-01No
5. Cables and wires	As required
6. CRO: dual trace	-01No
7. DMM	-01No
8. Bread board	-01No

Circuit Diagram:

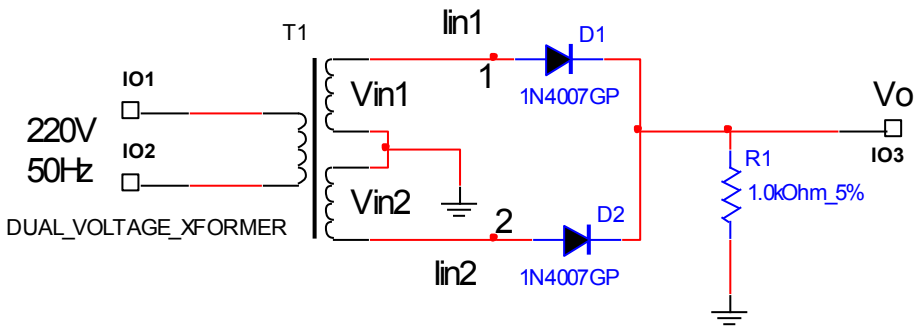


Fig3.1 Full wave rectifier

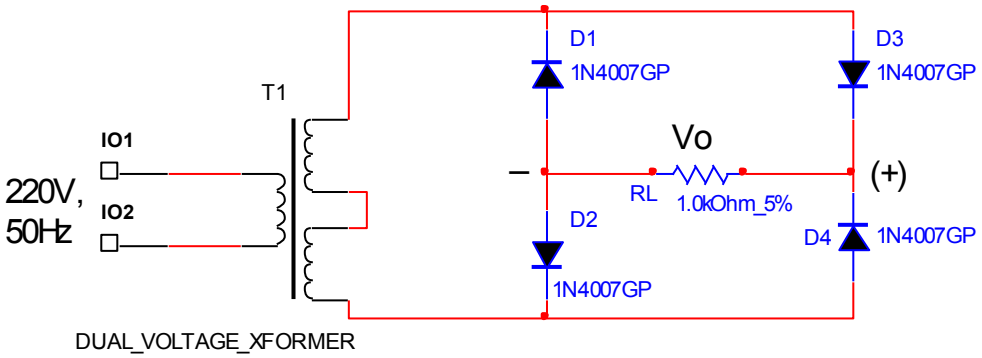


Fig3.2 Full wave Bridge Rectifier

Procedure:

1. Test the diodes using DMM and CRO.
2. Test the bridge rectifier using DMM and CRO
3. Note the color code on the resistor and record the resistor Type, Value, Tolerance and the Wattage.
4. Measure the resistors with the DMM and record.
5. Identify the centre tapped transformer input and output terminals.
6. Measure the resistance of the transformer secondary windings w.r.t. centre tap and total secondary resistance with the DMM and record.
7. Power the transformer. Observe, on the dual channel oscilloscope, the wave forms of the voltages of transformer secondary w.r.t the centre tap and record one below the other.

Full Wave Rectifier:

8. Connect the Circuit in Fig 3.1
9. Observe and record the wave forms of voltages $V_{in}1$, $V_{in}2$ and $V_{O;}$ one below the other with the CRO.
10. Measure the D.C Voltage and A.C Voltage of V_O with the DMM and record.
11. Calculate V_{DC} and V_{AC} from the wave forms noted in step9 and compare with the measured values of step10.
12. Calculate the ripple factor $r = \sqrt{(V_{AC} / V_{DC})^2 - 1}$

Half Wave Rectifier

13. Remove diode D_2 in the circuit in fig3.1
14. Repeat steps 9, 10, 11, and 12 for the half wave rectifier.

Bridge type full wave rectifier:

15. Connect the circuit in Fig 3.2
16. Observe the waveform V_O with the CRO and record
17. Repeat steps 10, 11, and 12 for the Bridge rectifier.

Post Lab:

1. Tabulate results V_{DC} and V_{AC} and the ripple factor for the three arrangements and compare their performance.
2. Compare the Experimentally obtained results with the theoretical results
3. From step 09 wave forms derive the waveform of $(V_{in1} - V_0)$ and $(V_{in2} - V_0)$ and note the peak value of the waveform. What is the significance of this waveform and the reading.
4. List the conclusions.

Questions:

1. What is the Frequency of the half wave rectifier output wave form?
2. What is the Frequency of the Full wave rectifier output wave form?
3. What is the Frequency of the Bridge rectifier output wave form?
4. How the secondary winding resistance of the Transformer and the dynamic resistance of the diode effect the performance
   of rectifier Circuits?
5. Explain how the following parameters can be determined for the rectifier circuits experimentally.
   a) Regulation b) Efficiency

EXPERIMENT: 04

HALF WAVE & FULL WAVE RECTIFIER CIRCUITS WITH CAPACITOR FILTER

Objectives:

To study the performance of

a) Half wave rectifier with capacitor filter

b) Full wave rectifier with capacitor filter

Pre lab:

4. Study the working of half wave & full wave rectifiers with capacitor filter and draw the expected waveforms.
5. Study the performance parameters of the half wave and full wave rectifiers with capacitor filter.
6. Study the data sheet of 1N4007 diode and note the maximum ratings.
7. Study the data sheet of W04M bridge rectifier and note the maximum ratings.

Components and Equipment:

1. Centre tapped step down 12-0-12V mains Transformer	-01 No
2. 1N4007 diodes	-02No
3. W04M Bridge Rectifier	-01 No
4. Capacitor Electrolytic 100µF, 63V	-01No
5. Resistor: Carbon 1K, 5%, 1/4W	-01No
6. Cables and wires	- As required
7. CRO: dual trace	-01No
8. DMM	-01No
9. Bread board	-01No

Circuit Diagram:

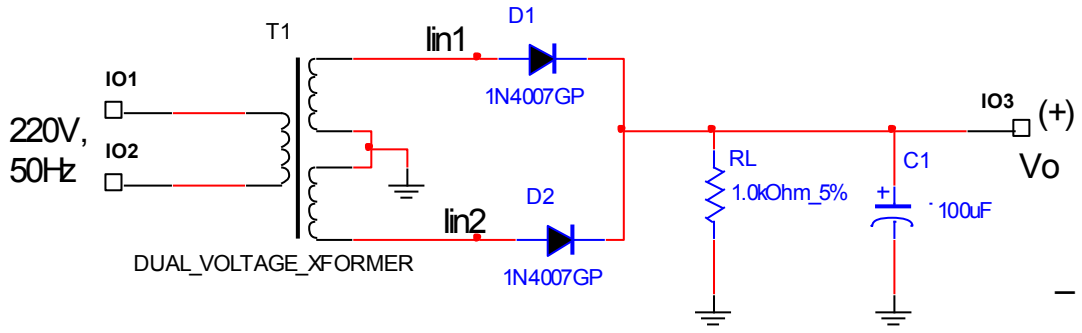


Fig4.1 Full wave rectifier with a Capacitor Filter

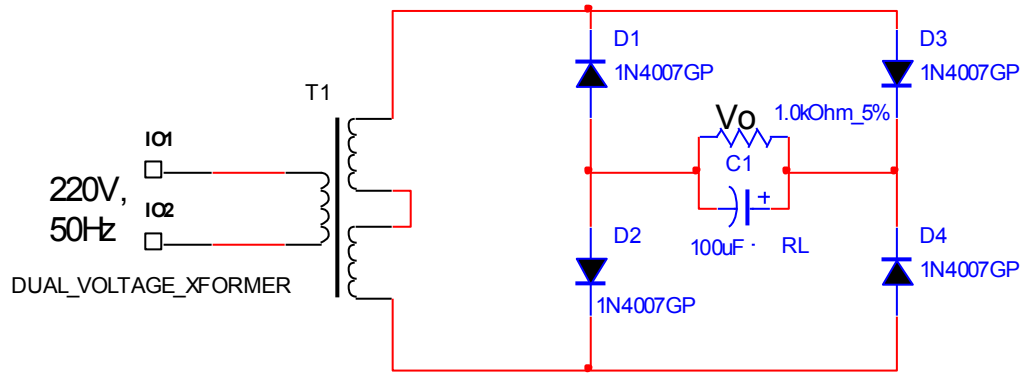


Fig4.2 Full wave Bridge Rectifier

Procedure:

1. Test the diodes using DMM and CRO.
2. Test the bridge rectifier using DMM and CRO
3. Note the color code on the resistor and record the resistor Type, Value, Tolerance and the Wattage.
4. Measure the resistors with the DMM and record.
5. Identify the centre tapped transformer output terminals.
6. Measure the resistance of the transformer secondary windings w.r.t. centre tap and total secondary winding resistance with the DMM and record.
7. Measure the capacitor value with the LCR meter and record the type of capacitor, value, voltage rating and tolerance.
8. Power the transformer. Observe, on the dual channel oscilloscope, the waveforms of the voltages of transformer secondary w.r.t the centre tap and record one below the other.

Full Wave Rectifier:

9. Connect the Circuit in Fig 4.1
10. Observe and record the waveforms of voltages $V_{in}1$, $V_{in}2$ and $V_{O;}$ one below the other with the CRO.
11. Measure the D.C Voltage and A.C Voltage of V_O with the DMM and record.
12. Calculate the ripple factor $r = \sqrt{[(V_{AC} / V_{DC})^2 - 1]}$
13. Remove the Capacitor in the circuit and repeat the steps 10, 11 and 12.

Half Wave Rectifier

14. Remove diode D_2 in the circuit in fig4.1
15. Repeat steps 9, 10, 11, and 12 for the half wave rectifier.

Bridge type full wave rectifier:

16. Connect the circuit in Fig 4.2

17. Observe the wave form V_O with the CRO and record

18. Repeat steps 11 and 12.

19. Remove the Capacitor in the Circuit and repeat the steps 11 and 12.

Post Lab:

1. Tabulate results V_{DC} and V_{AC} and the ripple factor for the three arrangements and compare their performance.

2. Compare the Experimentally obtained results with the theoretical results and explain the possible reasons for the difference.

3. List the conclusions.

Questions:

1. How can we enlarge the AC or ripple part of the output voltage V_O on the Oscilloscope screen.

2. What is the effect of the capacitor filter on the regulation characteristic of the rectifier.

3. How can performance of the circuits in terms of ripple factor be further improved? Suggest methods and explain.

4. How does the ripple vary with the variation of load R_L.

EXPERIMENT: 05

TRANSISTOR COMMON BASE CHARACTERISTICS

Objectives:

The objectives of this experiment are:

1. To plot the input characteristics of the BJT in common base configuration, i.e. to measure the emitter current I_E for different values
   of the Emitter-Base voltage V_{EB}, keeping the Collector - Base voltage V_{CB} constant.
2. To plot the output characteristics of the BJT in common base configuration, i.e. to measure the collector current I_C for different values
   of the Collector – Base voltage V_{CB}, keeping the emitter current I_E fixed.
3. To calculate from the characteristics the input dynamic resistance h_{ib}, output dynamic resistance($1/ h_{ob}$), the dc current gain h_{FB}
   (α_{DC}) and the small signal low frequency current gain h_{fb} (α_0) for the transistor at a typical operating point.
4. To identify on the output Characteristics the three regions of operation namely, the active or linear region the saturation and the
   cutoff regions.

Pre Lab:

1. Study the data sheets of 2N2222 and note the following

a) The type of the transistor.

b) The base diagram and identification of emitter base and collector.

c) The maximum ratings $V_{CBO,}$ $I_{C,}$ V_{EBO} and P_D.

d) Typical operating point.

e) Typical applications.

2. Sketch the theoretical input and output characteristics of a transistor in common base configuration and mark the three regions
   of operations on the output characteristics.
3. Define h_{ib}, $h_{fb\ and}$ h_{ob}, and distinguish between dc and small signal values.

Components and Equipment:

1.Transistor (2N2222)	---01no
2.Resistor (carbon 1KΩ, 5%,1/4 W)	----01no
3.Wires and cables	--- as required.

4.Bread board ---01 no.

5.DC voltage variable regulated power supply ----01no.

6.Digital multi meter (DMM) ----02no

7.Dual trace Oscilloscope ------01no.

Circuit Diagrams:

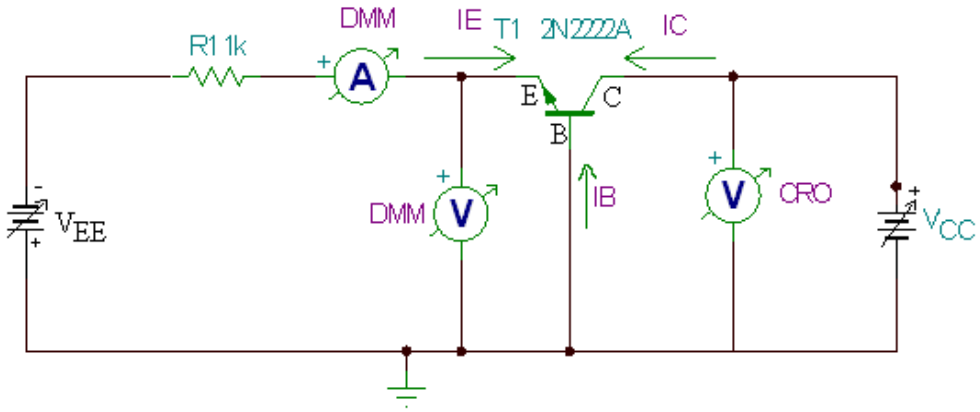


Fig 5.1 Circuit for Common Base Input Characteristics

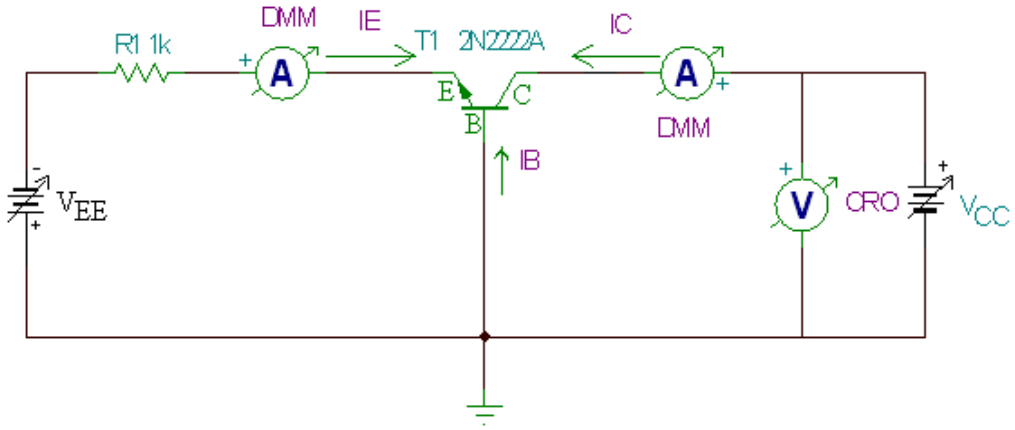


Fig 5.2 Circuit for Common Base Output Characteristics

Procedure:

1. Measure and note the exact value of the 1KΩ resistor with the DMM.
2. Measure and note h_{FE} of the transistor with the DMM.
3. Calculate h_{FB} **or** α_{DC} from the equation

$$\alpha_{DC} = h_{FB} = \frac{h_{FE}}{1+h_{FE}}$$

4. Connect the circuit in fig 5.1

Input Characteristics:

5. Maintain the voltage V_{CB} (V_{CC}) at 0V.
6. Increase V_{EE} from 0 to -10V in steps of -2V. At each step note I_E and V_{EB} in table 5.1
7. Repeat step 6 for V_{CB} at 5V and 10V.

Table 5.1 Common Base Input Characteristics Data

V_{CB} = 0V

I_E (mA)										
V_{BE} (mV)										

V_{CB} = 5V

I_E (mA)										
V_{BE} (mV)										

V_{CB} = 10V

I_E (mA)										
V_{BE} (mV)										

Output Characteristics:

8. Connect the circuit in fig 5.2

9. Leave the emitter terminal open without any input i.e. I_E = 0.Increase V_{CB} from 0 to 10V and note the collector current

$I_C(I_{CBO})$.

10. Connect the emitter terminal and set the emitter current to 1mA increasing V_{EE}.Increase V_{CB} from 0 to 10V in steps of 2V

and record I_C in table 5.2

11.Repeat step 10 for I_E =2, 4, 6, 8, and 10mA.

Table 5.2 Common Base Output Characteristics Data

I_E = 1mA

V_{CB} (V)	0	2	4	6	8	10		
I_C (mA)								

Post Lab:

1. Plot the input characteristics I_E Vs V_{EB} for different values of V_{CB}.

2. Plot the output characteristics I_C Vs V_{CB} for different values of I_E including I_E = 0.

3. From the input characteristics, calculate graphically at a typical operating point.

$$h_{ib} = \left.\frac{\Delta V_{EB}}{\Delta I_E}\right|_{V_{CB}\text{ constant}} \text{ ohms} \quad \text{and} \quad h_{IB} = \left.\frac{V_{EB}}{I_E}\right|_{V_{CB}\text{ Constant}} \text{ ohms}$$

4. From the output characteristics calculate graphically at a typical operating point

$$h_{fb} = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB}\ \text{constant}} \quad \text{and} \quad h_{FB} = \left.\frac{I_C}{I_E}\right|_{V_{CB}\ \text{constant}}$$

$$h_{ob} = \left.\frac{\Delta I_C}{\Delta V_{CB}}\right|_{I_E\ \text{constant}} \quad \text{and} \quad h_{OB} = \left.\frac{I_C}{V_{CB}}\right|_{I_E\ \text{constant}}$$

5. Compare h_{fb} with h_{FB} and h_{ob} with h_{OB}

6. Mark the three regions on the output characteristics.

Questions:

1 What is early voltage?

2 Explain how I_C flows even when $V_{CB} = 0V$.

3 Explain what happens when V_{CB} polarity is reversed and its effect on the output characteristics?

4 How can we calculate h_{rb} from the characteristics?

EXPERIMENT: 06

TRANSISTOR COMMON EMITTER CHARACTERISTICS

Objectives:

The objectives of this experiment are:

1. To plot the input characteristics of the BJT in common emitter configurations, i.e. to measure the base current I_B for different values of the Base –Emitter voltage V_{BE}, keeping the Collector-Emitter voltage V_{CE} constant.
2. To plot the output characteristics of the BJT in common emitter configurations, i.e. to measure the collector current I_C for different values of the Collector –Emitter voltage V_{CE}, keeping the Base current I_B fixed.
3. To calculate from the characteristics the input dynamic resistance h_{ie}, output dynamic resistance($1/ h_{oe}$), the dc current gain h_{FE} (β_{DC}) and the small signal low frequency current gain h_{fe} (β_0) for the transistor at a specified operating point.
4. To identify on the output Characteristics the three regions of operation namely, the active, the saturation and the cutoff regions.

Pre - Lab:

1. Study the data sheets of the transistor 2N2222 and note the following

a) The type of the transistor.

b) The base diagram and identification of emitter base and collector.

c) The maximum ratings $V_{CEO,}$ $I_{C,}$ $V_{BEO,}$ $P_{D,}$ and T_j.

d) Typical operating point.

e) Typical applications.

2. Sketch the theoretical input and output characteristics of a transistor in common emitter configuration and mark the three regions of operations on the output characteristics.
3. Define h_{ie}, h_{fe} , h_{re},and h_{oe}; and distinguish between dc and small signal values.

Components and Equipment:

1.Transistor (2N2222) --01no.

2.Resistor: Carbon 100KΩ, 5%,1/4 W --01no.

3.Wires and cables -- as required.

4.Bread board --01 no.

5.DC dual voltage variable regulated power supply ---01no.

6.Digital miltimeter (DMM) ----02no.

7.Dual trace Oscilloscope ----01no.

Circuit Diagrams:

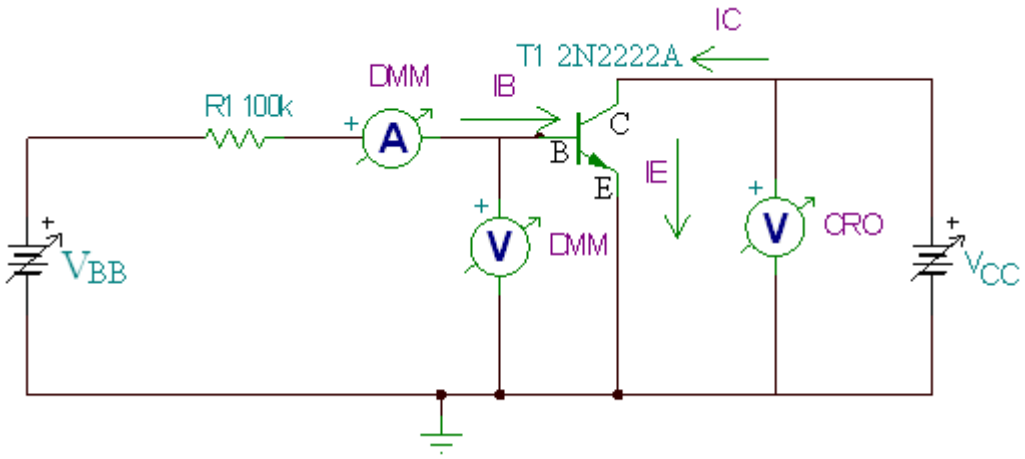


Fig 6.1 Circuit for Common Emitter Input Characteristics

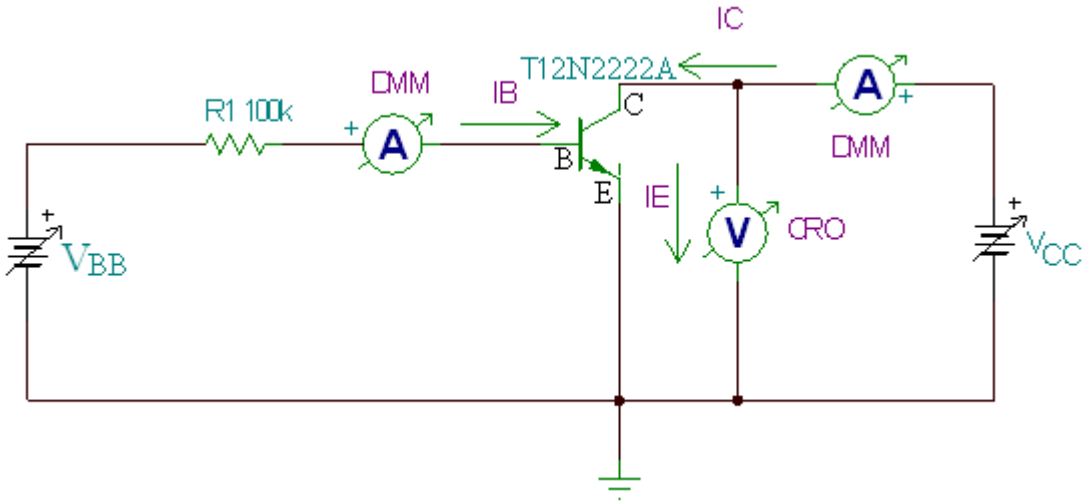


Fig 6.2 Circuit for Common Emitter Output Characteristics

Procedure:

1. Measure and note the exact value of the 100KΩ resistor with the DMM.
2. Measure and note h_{FE} of the transistor with the DMM.

Input Characteristics:

3. Connect the circuit in fig 6.1
4. Maintain the voltage V_{CE} at 0V.
5. Increase base current from 0 to 100µA in steps of 10µA; varying V_{BB} , and for each value of I_B note the base emitter voltage V_{BE} in table 6.1
6. Repeat step 5 for V_{CE} at 5V and 10V.

Table 6.1 Common Emitter Input Characteristics Data

V_{CE} = 0V (V_{CC} reduced to zero)

I_B (µA)	10	20	30	40	50	60	70	80	90	100
V_{BE} (mV)										

V_{CE} = 5V

I_B (µA)	10	20	30	40	50	60	70	80	90	100
V_{BE} (mV)										

V_{CE} = 10V

I_B (µA)	10	20	30	40	50	60	70	80	90	100
V_{BE} (mV)										

Output Characteristics:

7. Connect the circuit in fig 6.2
8. Leave the base terminal open without any input.
9. Increase V_{CE} from 0 to 10V in steps of 0.1V, 0.2V, 0.5V, 1V, 2V, 4V, 8V and 10V. For each value of V_{CE} note the collector current I_C (I_{CEO}) in table 6.2
10. Connect the base terminal and increase the base current in steps of 10, 20, 30,40,60,80 and 100 µA by increasing V_{BB} and repeat step 9 for each value of the base current. Tabulate the results in Table6.2

Table 6.2 Common Emitter Output Characteristics Data

I_B = 0 (base open)

V_{CE} (V)	0.1	0.2	0.5	1	2	4	8	10
I_C (I_{CEO}) mA								

I_B = 10µA

V_{CE} (V)	0.1	0.2	0.5	1	2	4	8	10
I_C (mA)								

Post Lab:

1. Plot the input characteristics I_B Vs V_{BE} for different values of V_{CE}.
2. Plot the output characteristics I_C Vs V_{CE} for different values of I_B including I_B = 0.
3. From the input characteristics calculate graphically at a typical operating point.

$$h_{ie} = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right|_{V_{CE}\text{ constant}} \quad \text{and} \quad h_{IE} = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right|_{V_{CE}\text{ constant}}$$

and compare the values.

4. From the output characteristics calculate graphically at a typical operating point

$$h_{fe} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}\text{ constant}} \quad \text{and} \quad h_{FE} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}\text{ constant}}$$

$$h_{oe} = \left.\frac{\Delta I_C}{\Delta V_{CE}}\right|_{I_B\text{ constant}} \quad \text{and} \quad h_{OE} = \left.\frac{\Delta I_C}{\Delta V_{CE}}\right|_{I_B\text{ constant}}$$

5. Compare h_{fe} with h_{FE} and h_{oe} with h_{OE}

6. Mark the three regions on the output characteristics.

Questions:

1. What is Early voltage? Obtain the same graphically from the output characteristics.

2. In common base arrangement I_C flows even when $V_{CBO} = 0$; but in common emitter arrangement $I_C = 0$ when $V_{CE} = 0$.

Explain.

3. The cutoff current,$I_{CEO,}$ in common emitter is much larger than I_{CBO} in common base. Explain

4. How can we identify or check the region in which transistor is operating?

5. What is the effect of temperature on the input and output characteristics of a transistor in common emitter configuration.

6. How can we calculate h_{re} from the characteristics ?

EXPERIMENT: 07

JUNCTION FIELD EFFECT TRANSISTOR CHARACTERISTICS

Objectives:

The objectives of this experiment are:

1. To plot the static output drain characteristics of the JFET.
2. To plot the static transfer characteristics of the JFET.
3. To verify the equation of the JFET

   $I_{DS} = I_{DSS} (1-V_{GS}/V_{PO})^2$ in the pinch-off region.

4. To determine the graphically from the characteristics the small signal parameters r_{ds}, g_m, and μ of the JFET.

Pre Lab:

1. Study the data sheet of the JFET BFW10/11 and note the following.
   a) The type of the JFET.
   b) The pin or base diagram of the JFET.
   c) Maximum ratings of V_{DS}, V_{GS}, P_D and T_J.
   d) I_{DSS}
   e) Typical operating point and the typical values of r_{ds} and g_m.
2. Draw the theoretical static output or drain characteristics of the JFET.
3. Draw the theoretical static transfer characteristics of the JFET.
4. Identify the three regions of operation on the output characteristics.
5. Define r_{ds}, g_m and μ and describe the procedure to obtain these parameters graphically from the Characteristics.

Components and Equipment:

1. JFET BFW10/11	---01no.
2. Resistor 33K, Carbon 1/4W, 5%	---01no.
3. Wires and cables	--- as required.
4. Bread board	---01no.
5. DC dual voltage regulated power supply	---01no.
6. Digital multi meter (DMM)	---01no.
7. Cathode Ray Oscilloscope (CRO)	---01no.

Circuit Diagram:

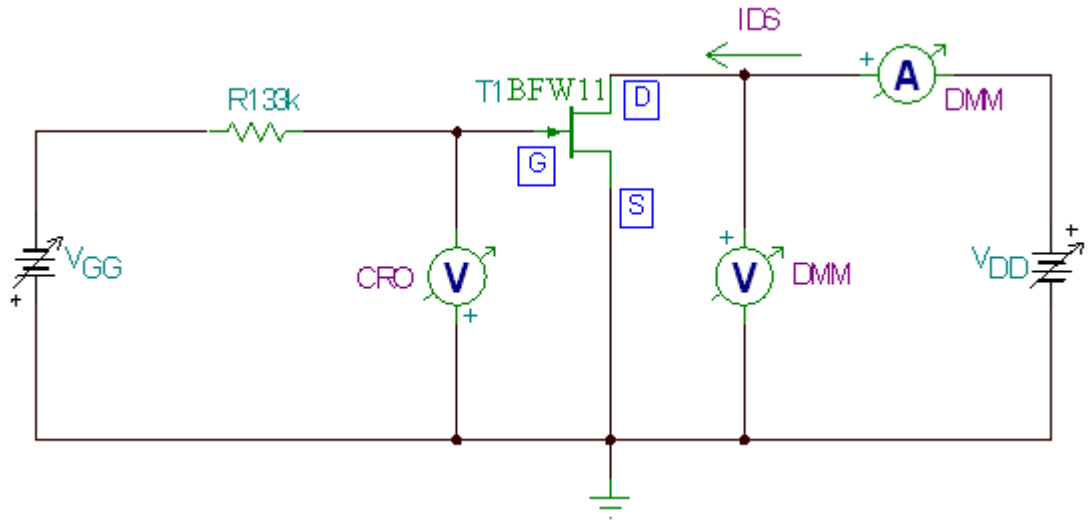


Fig 7.1 Circuit for the JFET Characteristics

Procedure:

1. Check the JFET functionality with DMM
2. Connect the circuit in fig7.1
3. Maintain the V_{GS} at zero volts. Increase V_{DS} from 0 to 10V in steps of 0V, 0.2V, 0.5V, 1V, 1.5V, 3V, 5V, 7V and 10V and note the Current I_{DS} for each value of V_{DS} and tabulate the readings in Table 7.1.
4. Repeat step 3 for V_{GS} = -0.5V,-1V, -1.5V, -2V, -3V and -5V.

Table 7.1 JFET output Characteristics Data

V_{GS} = 0

V_{DS} (V)	0	0.2	0.5	1V	1.5V	3V	5V	7V	10V
I_{DS} (mA)									

Transfer Characteristics:

5. Adjust V_{DS} to 6V.
6. Vary V_{GS} from 0 to -10V in steps of 1V and record I_{DS} at each step in table 7.2

Table 7.1 JFET Transfer Characteristics Data

V_{DS} = 6V

V_{GS}	**0**	**-1**	**-2**	**-3**	**-4**	**-5**	**-6**	**-7**	**-8**	**-9**	**-10**
I_{DS}											

Post Lab:

1. From the data in table 7.1 plot the set of output or drain characteristics I_{DS} vs V_{DS} for different values of V_{GS}.
2. From the data in table 7.2.plot the transfer characteristic I_{DS} vs $V_{GS.}$ Show that the data in table 7.2 satisfies the equation $I_{DS} = I_{DSS} (1-V_{GS}/V_{PO})^2$.
3. Select the operating pointing in the middle of the transfer characteristics and note for this point I_{DSQ} ,
V_{DSQ} and $V_{GSQ.}$
4. At the selected operating point calculate graphically the value of g_m from the transfer characteristics.
5. At the selected operating point calculate graphically the value of r_{ds} from the output characteristics.
6. At the selected operating current calculate graphically the value of 'μ'.
7. Compare the value of μ calculated graphically with the value obtained by multiplying g_m and r_{ds}.

Questions:

1. Distinguish between ohmic, pinch-off and cut-off regions of the JFET and the relationship between the current
and voltage relationship in each region.
2. "A JFET cut-off is pinched – off but the JFET pinched –off need not be cut-off" Explain.
3. Explain the function of 33K resistor in the circuit of fig7.1

EXPERIMENT: 08
SINGLE STAGE COMMON EMITTER BJT AMPLIFIER

Objectives:

The objective of this experiment is to calculate theoretically and verify practically the following performance parameters of a given BJT Amplifier.

1. The DC operating Point.
2. The maximum signal handling capacity of the amplifier, without any distortion of the output voltage.
3. The input impedance of the amplifier.
4. The output impedance of the amplifier.
5. The gain frequency response of the amplifier.

Pre lab:

1. Study data sheet of 2N2222 and note following :

a. The typical DC Operating Point

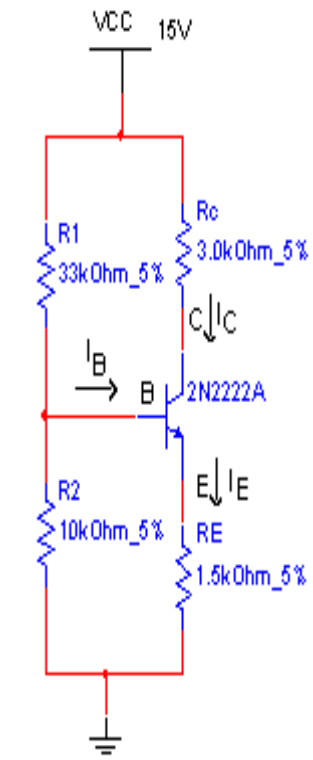
b. The h-parameters, h_{ie}, h_{re}, h_{fe} and hoe of the transistor.

2. Study the effect of the temperature changes on the operating point of the transistor and the need for the stability of the DC operating point.
3. Explain different types of biasing schemes and compare them.
4. Calculate the DC operating point of the Amplifier circuit in Fig. 8.1(a).
5. Draw the AC and DC load lines for the circuit in Fig.8.1(b) and estimate the maximum un-distorted peak to peak output signal amplitude.
6. From the h-parameters of the transistor calculate for the circuit in Fig.8.1(b) :
   i. The midband voltage gain
   ii. The input impedance of the amplifier
   iii. The output impedance of the amplifier
7. Sketch the Gain-Frequency plot of the amplifier.

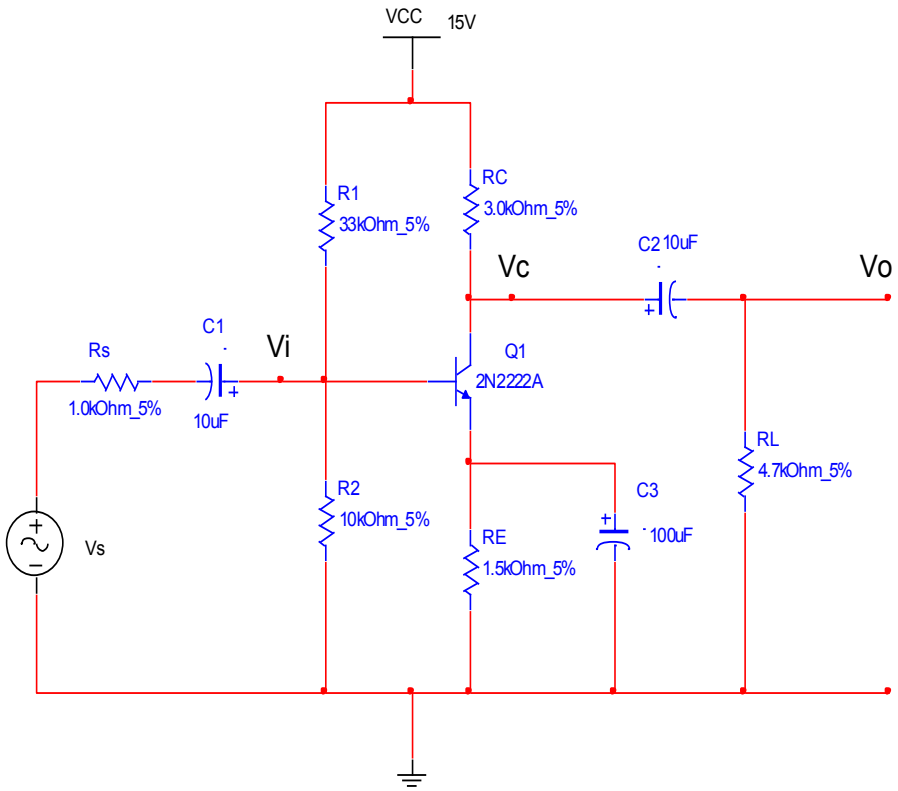
Components and Equipment:

Resistors :carbon, ¼ watt and 5% -1K, 33K, 10K, 3.3K, 1.5K and 4.7K one each
Capacitors: Electrolytic, 25V, 10%-10µF-2No's. and 100µF-1No.
Transistor: 2N2222 -1 No
Wires and cables – as required
Bread board – 1
Dual trace CRO – 1
DMM _ 1
DC variable regulated power supply 0-30V - 1

Circuit Diagram:



a) D.C Circuit



b) Complete Circuit

Fig 8.1 Single Stage Common Emitter BJT Amplifier

Procedure:

Operating Point:

1. Measure h_{FE} of the transistor with the DMM
2. Connect the circuit in Fig 8.1(a)
3. Measure the DC operating point VCEQ
4. Measure the Voltage across R_C and calculate I_{CQ}
5. Compare VCEQ & ICQ with the theoretically calculated values.

Maximum un-distorted signal:

6. Connect the circuit in Fig.8.2(b) and fix the function generator frequency at 5 KHZ
7. Connect the CRO at the output of the amplifier.
8. Increase the signal to the amplifier and observe the amplifier output waveform on the CRO. Increase the input until the output exhibits distortion and record the peak values of V_{smax} V_{imax} and V_{omax}

Gain –Frequency Response:

9. Adjust the amplifier signal input to a value below V_{smax} (say 50mV peak to peak).
10. Vary the input sine wave frequency from 10Hz to 1MHz in suitable steps and measure the output Voltage V_o of the amplifier at each step using CRO. Make sure the input voltage is kept constant throughout the frequency range.

Record the readings as shown in the tabular column

V_s =50mv (p-p) constant. V_i =

F	V_o(p-p)	$A_v=(V_o/V_i)$	Gain in dB =$20\log_{10} A_v$
10Hz 1MHz			

Input Impedance:

1. Adjust the input frequency to 5 KHz.
2. Measure and note V_s and V_i.

   Calculate $R_{in}= [V_i / (V_s-V_i)]*R_s$

Output Impedance:

3. Adjust the input frequency to 5 KHz.
4. Measure and note V_s, V_i and V_o.
5. Repeat step 14 without 4.7K (RL) and note V_s, V_i and V_{ONL}.
6. Calculate $R_o = [(V_{ONL}-V_o)/V_o]*R_L$.
7. Calculate the current gain:

   $Ai = i_L /i_{in} = [V_o/R_L] / [(V_s -V_i) / R_s]$

Post –lab

Compare experimentally obtained operating point, midband gain, maximum undistorted signal, Input and output Impedance and the current gain with the theoretically calculated values .Explain the discrepancies.

2 Plot the graph gain A_v vs frequency(f) on a semi-log graph paper.

3 Calculate the bandwidth of the Amplifier marking the bandwidth of the Amplifier; making the frequency points where the gain reduces to .707 of its maximum value.

Questions:

1 Why is a Semi-log Graph paper used for the plot ?

2 Why the gain reduces or falls at lower and higher frequencies ?

EXPERIMENT: 09
SINGLE STAGE COMMON SOURCE JFET AMPLIFIER

Objectives:

The objective of this experiment is to calculate theoretically and verify experimentally the following performance parameters of a given JFET Amplifier.

1. The DC Operating Point.
2. The maximum signal handling capacity of the amplifier, without distortion.
3. The output impedance of the amplifier.
4. The gain frequency response of the amplifier.

Pre lab:

1. Study the data sheet of JFET BFW10/11 and note the following :
   a. The type of JFET
   b. The pin or base diagram of the JFET
   c. The maximum rating of V_{DS}, V_{GS}, P_D, and T_j
   d. Values of I_{DSS} and V_{PO}
   e. Typical values of r_{ds} and g_m.
2. Study the effect of the temperature changes on the operating point of a JFET and the need for the stability of the DC operating point.
3. Explain different types of JFET biasing schemes and compare them.
4. Calculate the DC operating point I_{DSQ} and V_{DSQ} of the Amplifier circuit in fig 9.1 (a).
5. Calculate g_m of the JFET, at the Operating point calculated in step 4.
6. Draw the AC and DC load lines for the circuit in Fig.9.1(b) and estimate the maximum un-distorted peak to peak output signal amplitude.
7. Calculate the mid-band voltage gain of the amplifier.
8. Calculate the mid-band output impedance of the amplifier.
9. Sketch the Gain-Frequency plot of the amplifier.

Components and Equipment:

Resistors : carbon, ¼ watt and 5% -600Ω, 3K, 10K, 30K, and 150K - one each

Capacitors: Electrolytic - 100µF, 25V 1 No and 10 µF, 25V 2 No's.

FET : JFET BFW10/11 - 1No

Wires and cables – as required

DMM - 1 No.

Function generator -1 No.

DC power supply – 0-30V, 1A – 1No.

Circuit Diagram:

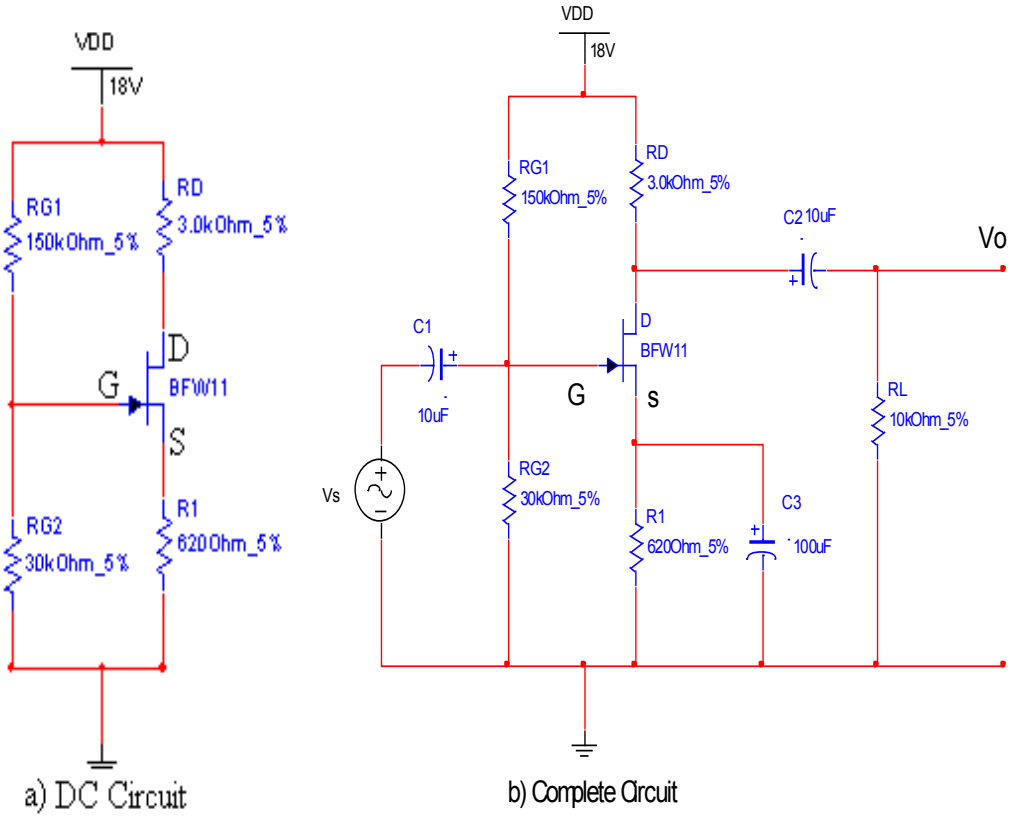


Fig 9.1 Single Stage Common Source JFET Amplifier

Procedure:

DC Operating Point:

1. Connect the circuit in Fig 9.1(a)
2. Measure V_{GSQ} and V_{DSQ}
3. Measure the Voltage across R_D and calculate I_{DSQ}
4. Compare V_{GSQ} & I_{DSQ} with the theoretically calculated values.

Maximum Un-distorted output signal:

5. Connect the circuit in Fig.9.1(b) and fix the frequency of the function generator at 5 KHZ
6. Connect the CRO at the output of the amplifier.
7. Increase the signal input to the Amplifier and observe the amplifier output waveform on the CRO. Increase the input until the output exhibits distortion and record the peak values

   V_{smax} V_{imax} and V_{omax}

Output Impedance:

8. Adjust the input signal amplitude to a value below V_{smax} in step 7
9. Measure and note V_s, and V_o.
10. Measure and note V_s, and V_{oNL} without R_L or 10K.
11. Calculate $R_o = [(V_{oNL}-V_o)/V_o]*R_L$.

Gain –Frequency Response:

12. Connect R_L and adjust the input signal amplitude to 50mv peak to peak.
13. Vary the input sine wave frequency from 10HZ to 1 MHZ in suitable steps and measure the output Voltage V_o at each step; using CRO. Make sure the input voltage ,Vs, is kept constant throughout the frequency range.

Record the readings in the tabular column as shown.

Vs= 50mvp-p constant, V_i =

Frequency (f)	V_o(p-p)	$A_v=(V_o/V_i)$	Gain in dB =20log $_{10}A_v$
10Hz …… ……. ……. . 1 MHz			

Post – lab

1. Compare experimentally obtained operating point, mid-band gain, maximum undistorted signal and the output impedance with the theoretically calculated values. Explain the discrepancies.
2. Plot the graph gain A_v vs frequency (f) on a semi-log graph paper.
3. Calculate the bandwidth of the amplifier; marking the frequency points, where the gain reduces to 0.707 of its maximum value.

Questions:

1. Why the gain reduces or falls at lower and higher frequencies.
2. Compare the BJT Common Emitter and FET Common Source amplifiers.

EXPERIMENT: 10
COMMON COLLECTOR BJT AMPLIFIER

Objectives:

The objective of this experiment is to calculate theoretically and verify practically the following performance parameters of a given BJT Amplifier in common collector configuration.

1. The DC Operating Point.
2. The maximum signal handling capacity of the amplifier, without distortion.
3. The input impedance of the amplifier.
4. The output impedance of the amplifier.
5. The small signal AC voltage gain at mid-band frequency.
6. The small signal AC current gain at mid-band frequency.
7. The voltage gain vs frequency response of the amplifier.

Pre lab:

1. Study the data sheet of 2N2222A and note the following :

a. The typical DC operating point.

b. The h – parameters; h_{ie}, h_{re}, h_{fe} and h_{oe} of the transistor.

2. Calculate the DC operating point of the amplifier circuit in Fig 10.1(a)

3. Draw the DC and AC Load lines for the circuit and estimate maximum un-distorted peak to peak output signal amplitude.

4. From the h – parameters of the transistor calculate for the circuit in Fig.10.1 (b) :

a. The input impedance.

b. The output impedance.

c. The mid-band voltage gain $A_v = V_o/V_i$.

d. The mid-band current gain $A_i = i_L / i_{in}$. and

e. The mid-band power gain $A_p = A_v.A_i$.

5. Sketch the voltage gain A_v vs Frequency plot of the amplifier.

Components and Equipment:

Resistors : carbon, ¼ watt and 5% -100Ω, 1.5 K, 3 K, 4.7 K and 33 K - one each and 10K – 2Nos.

Capacitors: Electrolytic -- 10µF, 25 V - 2 No and

100 µF 25 V - 2 No's.

Transistor -2N2222A -- 1 No.

Wires and cables – As required

CRO -- 1No.

DMM --1No.

Function generator --1.No.

Bread board – 1.No.

DC regulated power supply – 0-30V, 1A -1No.

Circuit Diagram:

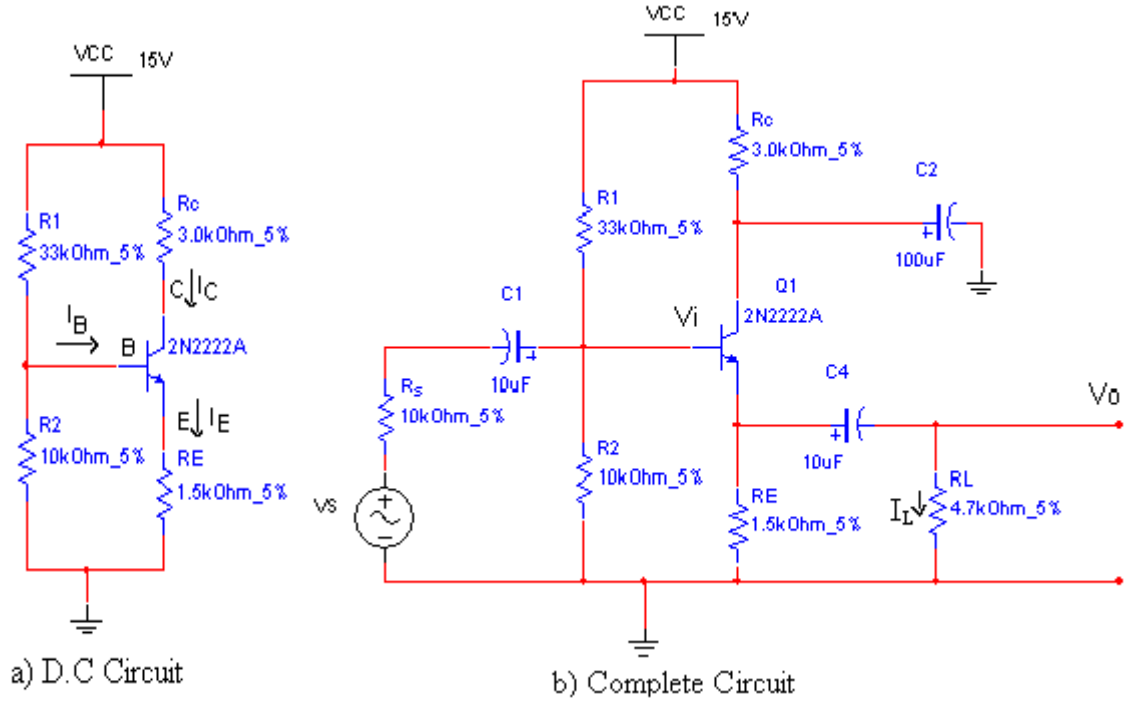


Fig 10.1 BJT Common Collector Amplifier.

Procedure:

DC Operating Point:

1. Measure h_{FE} of the transistor with the DMM
2. Connect the circuit in Fig 10.1(a)
3. Measure with DMM

   DC Voltages : V_C, V_E, V_B

   DC Currents : I_{CQ}, I_{EQ} and $I_{BQ.}$

   Calculate $V_{CEQ} = V_C - V_E$, $V_{BEQ} = V_B - V_E$ and $V_{CBQ} = V_C - V_B$.

   Calculate $h_{FE} = I_{CQ}/I_{BQ}$ and Compare with the value obtained in step 1.

Maximum un-distorted output signal:

4. Connect the circuit in Fig 10.1(b)
5. Connect CRO at the output of the amplifier.
6. Adjust the signal generator frequency to 5 KHz.
7. Increase the signal generator amplitude till the amplifier output develops distortion. Note the peak to peak values of V_{smax}, V_{imax} and V_{omax}.

Input and output Impedances:

8. Adjust the input signal amplitude V_s to a value below V_{smax} and frequency to 5KHz.
9. Measure and note V_s, V_i and V_o.
10. Measure $V_{o(NL)}$ without R_L; i.e 4.7K resistor.
11. Calculate $R_{in} = [V_i / (V_s - V_i)] * R_L$.

    $R_{out} = [V_{ONL} - V_o / V_o] * R_L$.
12. Calculate Current Gain $Ai = i_L / i_{in} = (V_o / R_L) / [(V_s - V_i) / R_s]$

Gain –Frequency Response:

13. Adjust the signal amplitude to a value below V_{smax} say 500mV PP.
14. Vary the input sine wave frequency from 10HZ to 1 MHZ in suitable steps (10, 20, 30, ……..100, 200, 400, 1K, 2K, 3K, 4K, 10K, 20K, 40K, 50K, 60K, 70K, 80K, 90K, 1M) and measure the output Voltage V_O of the amplifier at each step using CRO. Make sure the input voltage is kept constant at 500mV PP, throughout the frequency range.

    Record the readings as shown in the tabular column.

    Vs= 500mv (P-P) constant ; V_i =

Frequency (f)	V_o(p-p)	$A_v=(V_o/V_i)$	Gain in dB =20log $_{10}A_v$
10Hz 1MHz			

Post – lab

Compare the theoretically calculated values with the experimentally obtained results and explain the discrepancies.

Plot the graph gain A_v vs frequency f, on a semi-log graph paper.

Calculate the bandwidth of the amplifier; marking the frequency points, where the gain reduces to 0.707 of its maximum or mid frequency value.

Questions:

1. Compare the performance parameters of CE and CC arrangements.
2. What is the other popular name for the CC arrangement and why it is called so?
3. Where do we use CC amplifier Stage?

EXPERIMENT: 11
UJT CHARACTERISTICS

Objectives:

The objective of this experiment is:

1. The study the data sheet of the UJT.
2. The plot the emitter characteristics (V_E vs I_E).
3. To determine the intrinsic standoff ratio (η).

Pre lab:

1. Study data sheet of the UJT 2N2646 and note following :

a. Pin diagram

b. The maximum rating of :

Power dissipation $P_{D,}$

Max Emitter current I_E,

Maximum Emitter Reverse Voltage V_{B2E},

Maximum Inter-base Voltage V_{B2B1}.

c. Intrinsic standoff ratio (η).

2. Draw the UJT symbol and identify the terminals.
3. Draw the UJT VE vs IE Characteristic.
4. Briefly explain the UJT operation and identify important application.

Components and Equipment:

Resistors : carbon, ¼ watt and 5% -620Ω, 3K, 10K, 30K, and 150K ; one each

UJT : 2N2646-1No

Wires and cables – as required

Dual DC variable regulated power supply – 1

DMMs - 2

Circuit Diagram:

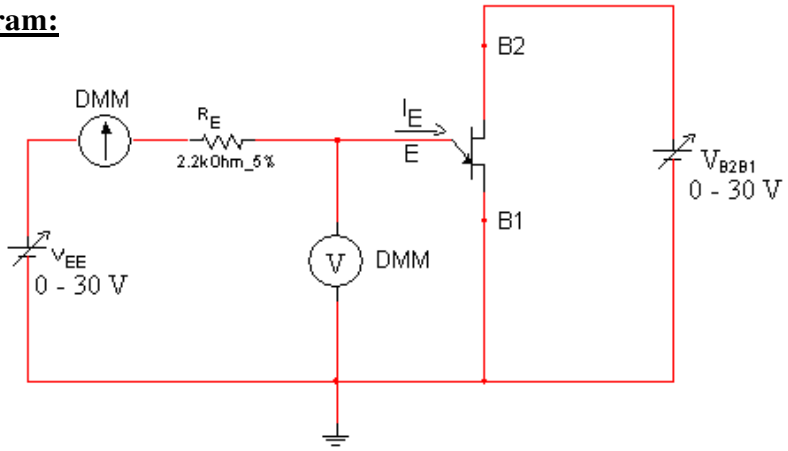


Fig 11. Circuit to Plot UJT Characteristics

Procedure:

Connect the circuit in Fig 11.

Adjust V_{B2B1} to 20 V.

Vary V_{EE} in steps of 1V from 0 to 30V and record current IE and voltage VE in the tabular column.

V_{B2B1} = 20V constant

Emitter Voltage VE in volts	Emitter Current IE in mA
1 2 3 .. .. 30 V	

4. Repeat the above steps for V_{B2B1} = 15 V constant value.

Post-Lab

1. Plot the V_E vs I_E for each value of V_{B2B1} and determine V_P for each value of V_{B2B1}.
2. Determine the Intrinsic standoff ratio ή from the equation

   $\eta = V_P / V_{B2B1}$
3. Note the valley voltage V_V from the characteristics plotted.

Questions:

1. Why UJT is called a negative resistance device and identify the negative resistance regular on the characteristics.
2. State whether the UJT characteristic is current controlled or voltage controlled and justifies your statement.

EXP.NO:12
SCR CHARACTERISTICS

Objectives:

The objectives of this experiment are:

1. To study the datasheet of the SCR.
2. To plot the V – I characteristics of the SCR.
3. To determine:

i. The forward – break over voltage, V_{BR}

ii. The Latching Current, I_L

iii. The Holding Current, I_H

iv. The on state resistance of the SCR

$$R_{ON} = \Delta V_{AK} / I_A$$

Pre lab:

1. Draw the SCR symbol and identify the terminals.
2. Study the datasheet of SCR, BT 169, and note the pin diagram and maximum ratings.
3. Sketch the static characteristics of the SCR and mark the following on the characteristics

a. Forward – break over voltage

b. Holding Current

c. Latching Current

d. Forward Current

e. Gate Current

f. Reverse – breakdown voltage

g. Forward conduction region

h. Forward blocking and reverse blocking regions

4. Mention important application of SCR.

Components and Equipment:

SCR – BT169 – 1No

Resistors – Wire wound type 100Ω – 10w – 1No

Metal Film type 1000 Ω - 1w – 1No

Wires and Cables – as required

DMMS – 2Nos

CRO – 1No

Dual DC regulated supply – 0 to30V – 1No

Circuit Diagram:

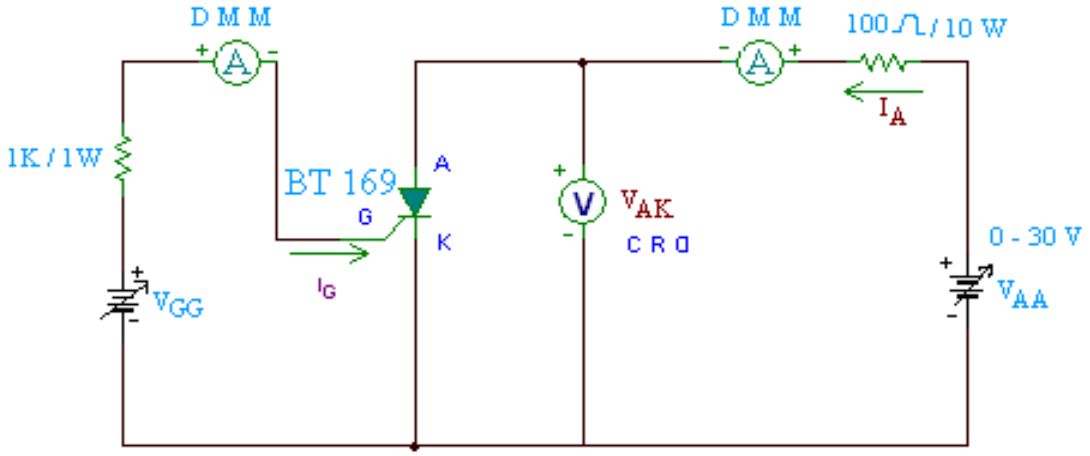


Fig 12.1 Circuit to Plot SCR Static Characteristics.

Procedure:

1. Connect the circuit in fig12.1.
2. Adjust V_{AA} and I_G to Zero.
3. Maintain I_G = 0 and increase V_{AA} in steps and record the readings in the tabular column.

$I_G = 0$

V_{AA} (V)	5	10	15	20	25
V_{AK} (V)					
I_A (mA)					

Repeat step 3 for I_G = 5mA

$I_G = 5mA$

V_{AA} (V)	5	10	15	20	25
V_{AK}(V)					
I_A (mA)					

4. Increase V_{AA} slowly, for I_G = 5mA, from zero and note the voltage at which V_{AK} suddenly falls and the corresponding value of I_A; i.e. the forward break over voltage V_{BO} and the SCR holding Current I_H for I_G = 5mA.
5. Open the gate when the SCR is conducting with the maximum value of V_{AA}. Reduce slowly the voltage V_{AA} and note the Latching Current I_L (I_A) when the SCR switches off or the voltage V_{AK} suddenly increases. The Latching Current I_L is always higher than the Holding Current I_H.
6. Repeat steps 4, 5 and 6 for I_G = 10mA and I_G = 15mA and tabulate your results. Record Holding Current I_H and Latching Current I_L in each case.

Post-Lab

1. Plot the I_A vs V_{AK} Characteristics of the SCR for different values of I_G.
2. Mark on the characteristics the forward break over voltage, holding current and the Latching current.
3. Determine the dynamic or the ON-State resistance of the SCR from the characteristics.
4. Mark the negative resistance region in the characteristic.

Questions:

1. Define breakdown voltage, holding current, latching current and the on state resistance of an SCR.
2. Write an expression for the anode current.